IN THE CLAIMS

Please amend claims 1, 31, and 38 as indicated below.

1. (Currently Amended) An apparatus, comprising:

a memory unit to store data;

a plurality of memory-sensing devices coupled to the memory unit to sense the data stored in the memory unit substantially concurrently;

a request queue coupled to the memory unit via the memory-sensing devices, the request queue storing one or more requests while the memory-sensing devices are sensing data in the memory unit;

a response queue coupled to the memory-sensing devices, the response queue storing data from the memory-sensing devices that is not required to be returned to a requester immediately; and

an arbiter coupled to said response queue to transmit one or more responses stored in the response queue to a requester in an order based on a priority of the respective request corresponding to the response,

wherein the one or more requests include a first request from a first requester for requesting data having a first portion and a second portion and a second request from a second requester received after the first request for requesting data having a first portion and a second portion, and wherein the first portion of the second request is returned to the second requester before the second portion of the first request is returned to a first requester.

2. (Previously Presented) The apparatus of claim 1, wherein the memory-sensing devices comprise redundant circuitry capable of sensing data in the memory unit independently and substantially simultaneously.

3. (Original) The apparatus of claim 1, wherein said request queue comprises memory to store more than one request.

4. (Original) The apparatus of claim 3, wherein the memory to store more than one request comprises memory to service more than one request substantially simultaneously.

5. (Original) The apparatus of claim 1, wherein said response queue comprises memory to store data for a response.

6. (Original) The apparatus of claim 1, wherein said arbiter comprises a response arbiter to determine a response to more than one request.

7. (Previously Presented) The apparatus of claim 6, wherein the response arbiter comprises a priority determiner to determine a priority of a response to a request, wherein a response having a higher priority is returned to the requester prior to a response having a lower priority.

8. (Previously Presented) The apparatus of claim 6, wherein said arbiter comprises a request arbiter coupled to said request queue, wherein the request arbiter transmits a request having a higher priority to a memory-sensing device prior to transmitting a request having a lower priority.

9. – 30. (Canceled)

31. (Currently Amended) An apparatus, comprising:

a memory unit to store data;

a plurality of memory-sensing devices coupled with said memory unit, the plurality of memory-sensing devices capable of sensing data stored in the memory unit substantially concurrently;

a request queue coupled with said memory sensing devices to receive more than one request to sense data in said memory unit; and

an arbiter coupled with said memory sensing devices to determine the sequence to return the data in response to the more than one request, the data being returned in an order based on a priority of the respective request determined by the arbiter.

wherein the more than one request includes a first request from a first requester for requesting data having a first portion and a second portion and a second request from a second requester received after the first request for requesting data having a first portion and a second portion, and wherein the first portion of the second request is returned to the second requester before the second portion of the first request is returned to a first requester.

32. (Previously Presented) The apparatus of claim 31, further comprising a response queue coupled with said memory sensing device to store the data prior to the arbiter returning the data in the order based on the priority of the corresponding request.

33. (Previously presented) The apparatus of claim 31, wherein said memory unit comprises a first partition and a second partition; and said memory-sensing device comprises redundant circuitry coupled with said memory unit to sense data in the first partition and the second partition substantially simultaneously.

34. (Previously presented) The apparatus of claim 31, wherein said request queue comprises memory to store the more than one request.

35. (Previously presented) The apparatus of claim 31, wherein said arbiter comprises a response arbiter coupled with said memory sensing device to determine a response to the more than one request.

36. (Previously presented) The apparatus of claim 35, wherein the response arbiter comprises a priority determiner to determine a priority of the response to the more than one request.

37. (Previously presented) The apparatus of claim 31, wherein said arbiter comprises a request arbiter coupled with said request queue to determine a priority to sense data in response to the more than one request.

38. (Currently Amended) A system, comprising:

a processor; and

a memory device coupled to the processor, the memory device including

a memory unit to store data,

a plurality of memory-sensing devices coupled with said memory unit to sense the data stored in the memory unit substantially concurrently,

a request queue coupled with said memory sensing devices to receive more than one request to sense data in said memory unit, and

an arbiter coupled with said memory sensing devices to determine the sequence to return the data in response to the more than one request based on a priority of the requests determined by the arbiter,

wherein the more than one request includes a first request from a first requester for requesting data having a first portion and a second portion and a second request from a second requester received after the first request for requesting data having a first portion and a second portion, and wherein the first portion of the second request is returned to the second requester before the second portion of the first request is returned to a first requester.

39. (Previously presented) The system of claim 38, further comprising a memory controller coupled between said request queue and said processor.

40. (Previously presented) The system of claim 38, further comprising an input-output device.

41. (Previously Presented) The apparatus of claim 8, wherein the one or more requests include a first request for non-critical data and a second request received after the first request

for critical data, and wherein the second request is transmitted to an idle memory-sensing device prior to the first request.

42. (Previously Presented) The apparatus of claim 41, wherein if no idle memory-sensing device is available, the request arbiter stores the first and second requests in the request queue in an order, such that the second request is processed prior to processing the first request when an idle memory-sensing device becomes available.

43. (Previously Presented) The apparatus of claim 42, wherein the request arbiter marks the second request having a higher priority than the first request when storing the first and second requests in the request queue.

44. (Previously Presented) The apparatus of claim 41, wherein in response to the first and second requests, the critical data and the non-critical data are stored in the response queue in an order, such that the critical data is turned to the respective requester prior to returning the non-critical data.

45. (Previously Presented) The apparatus of claim 44, wherein the critical data is stored in a dedicated area of the response queue, and wherein data in the dedicated area of the response queue is returned to the respective requester prior to returning data in a remaining area of the response queue.

46. (Previously Presented) The apparatus of claim 44, wherein the critical data stored in the response queue is associated with a tag indicating to the response arbiter that the associated data should be returned in a relatively high priority.

47. (Previously Presented) The apparatus of claim 8, wherein the one or more requests include a first request for a first data having a critical portion and a non-critical portion, and a second request received after the first request for a second data having a critical portion and a non-critical portion, and wherein the critical portions of the first and second requests are processed by one or more idle memory-sensing devices prior to processing the non-critical portions of the first and second requests.

48. (Previously Presented) The apparatus of claim 47, wherein if no idle memory-sensing device is available, the request arbiter stores the first and second requests in the request queue in an order, such that the critical portions of the first and second requests are processed prior to processing the non-critical portions when an idle memory-sensing device becomes available.

49. (Previously Presented) The apparatus of claim 48, wherein the request arbiter marks the critical portions of the first and second requests having a higher priority than the non-critical portions when storing the first and second requests in the request queue.

50. (Previously Presented) The apparatus of claim 47, wherein in response to the first and second requests, the critical data and the non-critical data are stored in the response queue in

an order, such that the critical data is turned to the respective requester prior to returning the non-critical data.